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(71) Applicant: APPLIED MATERIALS, INC. [US/US]; P.O. Box 450 A, Santa Clara, CA 95052 (US).

(72) Inventors: KUMAR, Ajay; 510 Kemilworth Court, Sunnyvale, CA 94087 (US). KHAN, Anisul; 125 Conemara Way #85, Sunnyvale, CA 94087 (US). LIU, Wei; 936 Azure Street #A12, Sunnyvale, CA 94087 (US). CHAO, John; 1482 Fields Drive, San Jose, CA 95129 (US). CHINN, Jeff; 605 St. Croix Lane, Foster City, CA 94404 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).

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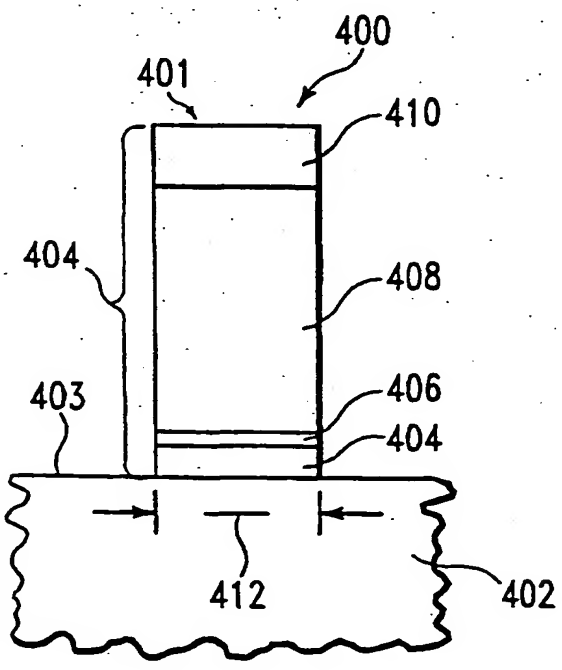

(57) Abstract: The present disclosure provides a method for etching trenches, contact vias, or similar features. The method requires the use of a metal-comprising masking material in combination with a fluorine-comprising plasma etchant. The plasma feed gas includes at least one fluorine-containing compound such as nitrogen trifluoride (NF_3), carbon tetrafluoride (CF_4), and sulfur hexafluoride (SF_6). Oxygen (O_2), or an oxygen-comprising compound, or hydrogen bromide (HBr), or a combination thereof may be added to the plasma feed gases.

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METAL MASK ETCHING OF SILICON

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention pertains to a method for plasma etching deep trenches, typically at least 50 _m deep, into a silicon substrate while maintaining control over the sidewall profiles which border the trench.

2. BRIEF DESCRIPTION OF THE BACKGROUND ART

In semiconductor device fabrication, it is frequently desirable to create deep trenches in a silicon substrate. Typically silicon dioxide has been used as a masking material for plasma etching of trenches in an underlying silicon substrate. The plasma etch selectivity of silicon relative to silicon oxide, i.e. the ratio of the silicon etch rate to the silicon oxide etch rate, is up to about 40 : 1, depending on the composition of the plasma etchant. The trench is typically etched in a silicon substrate using a plasma feed gas comprising chlorine, or oxygen, or a combination thereof. The plasma feed gas may include small amounts of SF_6, added for profile control.

While 40 : 1 selectivity is acceptable for a number of fabrication applications, such as gate type field effect transistors, it is not adequate for many micromachining applications, or for fabrication of deep trench capacitors, deep trench isolation (DTI) for high frequency circuitry, power devices, and numerous other applications. For example, with respect to especially deep trenches of the kind required for deep trench capacitors used in DRAM cells where the trench may be 200 _m deep, a 40 : 1 selectivity would require a silicon oxide mask thickness of about 5 _m, which causes numerous problems. Use of such a thick masking layer of silicon oxide makes it more difficult to control the sidewall profile of the trench as it is etched; since, as etching progresses the edges of the masking layer above the opening are eroded away and the shape at the top of the opening changes.

It is highly desirable to have a thin masking layer which has a sufficiently low etch rate compared to that of silicon that the selectivity is extended beyond 40 : 1.

SUMMARY OF THE INVENTION

The present invention provides a method for etching trenches, contact vias, or similar features to a depth of 100 _m and greater while permitting control of the etch profile (the shape of the sidewalls surrounding the etched opening). The method requires the use of a metal-comprising masking material in combination with a fluorine-comprising plasma etchant. The byproduct produced by a combination of the metal with reactive fluorine species must be essentially non-volatile under etch process conditions, and sufficiently non-corrosive to features on the substrate being etched, that the device features remain unharmed by the etch process. By unharmed it is meant that performance of a semiconductor device feature in the substrate is not affected, or that any residue from the etch process that could affect feature performance can be removed to leave the device feature essentially unaffected.

Although aluminum is a preferred metal for the metal-comprising mask, since aluminum is already present in most semiconductor processing chambers and the effect produced by the presence of aluminum in most semiconductor processes is known, other metals can be used for the masking material, so long as they produce an essentially non-volatile, non-corrosive etch byproduct under etch process conditions. By way of example, and not by way of limitation, metallic materials recommended for the mask include aluminum, cadmium, copper, chromium, gallium, indium, iron, magnesium, manganese, nickel, and combinations thereof. In particular, aluminum in combination with copper or magnesium is particularly useful, where the copper or magnesium content is less than about 8 % by weight, and other constituents total less than about 2 % by weight.

The plasma feed gas includes at least one fluorine-containing compound such as nitrogen trifluoride (NF_3), carbon tetrafluoride (CF_4) , sulfur hexafluoride (SF_6), silicon tetrafluoride (SiF_4), trifluoro methane (CHF_3), difluoro methane (CH_2F_2) and perfluoro 1-butene, or perfluoro 2-butene, or perfluro cyclobutane (C_4F_8), by way of example and not by way of limitation.

Oxygen, or an oxygen-comprising compound may be added to the plasma feed gases to help provide a protective layer over etched sidewalls, assisting in profile control of the etched feature. The preferred atomic ratio of oxygen : fluorine in the plasma feed

gas ranges from about 0.25 to about 0.50. Plasma feed gases comprising CH_2F_2 and SF_6, and O_2; or comprising C_4F_8 and SF_6, and O_2 work well, for example and not by way of limitation.

The addition of hydrogen bromide (HBr) to the plasma feed gas also helps protect sidewall integrity. And, although the non-HBr chemistries mentioned above work well, they are compound depositing in nature, so that a combination of HBr with SF_6 and O_2, for example provides a cleaner process and is preferred.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of an individual polysilicon etch chamber 102 of the type used in an Applied Materials' CENTURA® DPS Plus™ silicon etch system, which is a preferred example of an etch processing apparatus for performing the method of the invention.

Figure 2 shows a cross-sectional side view of the silicon etch chamber 102 shown in Figure 1.

Figure 3A shows a schematic of a cross-sectional view 300 of the Example One etch structure, consisting of a silicon substrate having an aluminum mask of lines and spaces deposited thereover. The aluminum mask lines 304 rest on the upper surface 303 of the silicon substrate302.are shown as

Figure 3B shows the etch structure of Figure 3A after completion of etch.

Figure 3C shows the etch structure of Figure 3B after a clean-up procedure in which the etched structure is dipped in a dilute HF solution to remove residual oxides from the surface of the structure.

Figure 4A shows a schematic of a cross-sectional view 400 of the Example Two etch structure, consisting of a pattern of lines 404 resting on the upper surface 403 of a single crystal substrate 402. In the area of lines 404, the single crystal silicon substrate 402 upper surface 403 has a layer of TEOS 404 in direct contact with upper surface 403, a layer of Si_3N_4 406 overlying the TEOS layer404,, a masking layer 408 of Al-Cu overlying the Si_3N_4 layer 406, and a second TEOS layer 410 overlying the Al-Cu masking layer 408.

Figure 4B shows a schematic of a photomicrograph taken after etching of the film

structure 400 shown in Figure 4A, where a portion of Al- Cu masking layer 408 a has been plasma etched, while another portion 408 b has been protected from the etchant plasma. The line 404 etched into silicon substrate 404 is considerably wider at the Al-Cu masking layer than at the base of the etched silicon 417, i.e. the line sidewall profile is significantly undercut.

Figure 4C is a graph showing the change in silicon etch rate as a function of the bias applied to the etch structure during etching.

Figure 4D is a graph showing the change in selectivity (ratio of the etch rate of silicon to the etch rate of the aluminum masking material) as a function of the bias applied to the etch structure during etching.

Figure 5 is a schematic of an apparatus for carrying out method of invention, including a control system.

DETAILED DESCRIPTION OF THE INVENTION

1. DEFINITIONS

As a preface to the detailed description, it should be noted that, as used in this specification and the appended claims, the singular forms "a", "an", and "the" include plural referents, unless the context clearly dictates otherwise. Thus, for example, the term "semiconductor" includes a variety of different materials which are known to have the behavioral characteristics of a semiconductor, reference to a "metal" or "metallic" masking material includes metals such as aluminum, cadmium, copper, chromium, gallium, indium, iron, manganese and nickel, as well as other conductive materials which would be suitable in the application described.

Specific terminology of particular importance to the description of the present invention is defined below.

The term "bias power" refers to, but is not limited to, the power applied to a substrate to increase the attraction of ions toward a substrate, thereby increasing the anisotropicity of a plasma etching process.

The term "etch structure", "etch stack" or "film stack" refers to a collection of layers of different materials deposited one over the other, at least a portion of which are etched during an etching process.

The term "etch profile"or "feature profile" generally refers to, but is not limited to, the cross-sectional profile of the sidewall of an etched feature. In many instances herein, the etch profile is described in terms of an angle between the sidewall and the surface on which the feature stands (*i.e.*, the substrate). The term "vertical profile" refers to a feature profile wherein a cross-section of the feature exhibits sidewalls which are perpendicular to the surface on which the feature stands. The term "reentrant profile" (also known as an "undercut" profile) refers to a feature profile wherein the width of the cross-section of the feature is larger as the distance away from the opening on the substrate increases. The term "tapered" profile refers to a feature profile wherein the width of the cross-section of the feature is smaller as the distance away from the opening on the substrate surface increases.

The term "feature" refers to, but is not limited to, contacts, vias, trenches, and other structures which make up the topography of the substrate surface.

The term "feature size" typically refers to the smallest dimension of a feature (*i.e.*, the shortest distance between the sidewalls of a feature).

The term "selectivity" or "etch selectivity" is used to refer to (a) a ratio of etch rates of two materials; and (b) a condition achieved during etch when etch rate of one material is increased in comparison with another material.

The term "source power" refers to the power that is responsible for sustaining the plasma and providing the energy to high energy species in the chamber.

The term "substrate" includes semiconductor materials, glass, ceramics, polymeric materials, and other materials of use in the semiconductor industry.

2. AN APPARATUS FOR PRACTICING THE INVENTION

The present invention may be practiced in any apparatus adapted to expose a substrate to a plasma. Preferably the apparatus is capable of applying a bias voltage to the substrate. An apparatus which has provided excellent results employs an inductively coupled plasma, where a power supply to an inductive coil and a power supply to bias the substrate are independently controlled. This enables the selection of a desired plasma density independently of the selection of the amount of energy with which ion

bombardment occurs upon the substrate surface.

However, the present invention may be practiced in an apparatus having a plasma source power and bias power which are not separately controllable, or in any other type of apparatus adapted to expose a substrate to a plasma.

The CENTURA® DPS Plus™ silicon etch system available from Applied Materials, Inc. of Santa Clara, California is an example of a system which provides independent control of the source power supply and the bias power supply.

Figures 1 and 2 are schematics of an individual CENTURA® DPS Plus™ silicon etch chamber 102 of the type used in the Applied Materials' CENTURA® silicon etch system. The CENTURA® DPS Plus™ polysilicon etch chamber 102 is configured to be mounted on a standard CENTURA® 5200 etch mainframe. The polysilicon etch chamber 102 comprises an upper chamber 104 having an internal ceramic dome 106, and a lower chamber 108. The lower chamber 108 includes a monopolar electrostatic chuck (ESC) cathode 110. Gas is introduced into the chamber via ceramic gas injection nozzles 114. Chamber pressure is controlled by a closed-loop pressure control system 118 with a throttle valve 116.

Figure 2 shows a schematic of a cross-sectional side view of a polysilicon etch chamber 102. During processing, a substrate 220 is introduced into the lower chamber 108 through inlet 222. The substrate 220 is held in place on the surface of electrostatic chuck (ESC) cathode 110 by applying a DC voltage to a conductive layer (not shown) located under a dielectric film (not shown) on the chuck surface. The cathode 110 and substrate 220 are raised by a wafer lift 224 and so that cathode 110 and substrate 220 are raised into position for processing. Etch gases are introduced into the upper chamber 104 via the ceramic gas injection nozzles 114. The polysilicon etch chamber 102 employs an inductively coupled plasma generated using inductive coil 234, to which power is applied via power source 226 and matching network 228 operating at substantially 12.56 MHZ. A high density plasma can be generated and sustained using this apparatus. The wafer 220 is biased by application of power applied through cathode 110 via an RF source 230 and matching network 232 operated at substantially 13.56 MHZ. The plasma source power 226 and substrate biasing via RF source 230 are controlled by separate controllers (not shown). When an etch end point is evidenced by

etching to an interface between two different materials, an endpoint subsystem (not shown) senses the end of the etch process by monitoring changes in the light emitted by the plasma in the etch chamber 102.

3. THE METHOD FOR METAL MASK ETCHING OF SILICON

As previously mentioned, silicon is typically plasma etched using a plasma feed gas comprising chlorine and oxygen. However, the etchant species provided by this plasma feed gas provide an etch selectivity of silicon relative to silicon oxide which is in the range of about 40 : 1. To etch a trench 300 _m deep, the silicon oxide etch mask must be at least 7.5 _m (75,000 _) thick. Use of such a thick mask creates very significant stress on the underlying substrate surface; the silicon oxide mask itself may crack from the stresses created at such thicknesses. These factors, and others, make the use of a mask of this thickness economically impractical. To improve the selectivity of silicon relative to the masking material, a number of different masking materials were considered. We decided to investigate the use of metal-comprising masking materials.

A useful metal-comprising masking material etches slowly in comparison to the silicon etch rate, and the etch byproducts formed should not harm the etched semiconductor structure or features contained therein. We have discovered that if the etch byproducts from the metal-comprising masking material are sufficiently nonvolatile, they can be used to limit the etch rate of the masking material, providing an etch selectivity of silicon relative to the metal-comprising masking material which is significantly better than 40 : 1. When a major component of the metal-comprising masking material is aluminum, we have determined that the reaction by-product between a fluorine-comprising etchant and the aluminum helps reduce the etch rate of the aluminum-comprising masking material and is substantially non-corrosive, providing an advantageous etch process. The etch byproduct of aluminum and chlorine etchant species is too volatile to sufficiently reduce the aluminum-comprising mask etch rate. Iodine etchant species were not selected due to the difficulty in handling iodine and the volatility of the by-product formed from the aluminum-iodine species reaction. The etch byproduct of aluminum with bromine is very corrosive. It is particularly helpful that the aluminum fluoride (AlF_3) byproduct melting point at standard conditions is about 1290

_C, at which temperature it sublimes (reducing any potential for corrosion). One skilled in the art, using published handbooks which provide physical and chemical property data for metal compounds, can select combinations of other metals with known-in -the -art etchants to arrive at metal/etchant byproducts which are highly likely to provide the desired non-volatility and non-corrosive properties to function within the description of the present invention.

EXAMPLE ONE :

Eight individual etch experiments were carried out in this Example. The substrate wafer size was 200 mm, and the wafer was notched. Three wafers were available, and to obtain maximum information using a single wafer, portions of the wafer were protected during an etch process, so that a wafer could be reused. The etch process was performed in a CENTURA® DPS Plus™ polysilicon etch chamber of the kind previously described. This etch chamber was equipped with a heat exchanger to control the dome and wall temperature and a separate heat exchanger to control the temperature of the electrostatic chuck cathode upon which the wafer substrate rested.

Figure 3A shows a schematic of a cross-sectional view of a film structure for a wafer portion 300 which was etched. The substrate 302 was single crystal silicon. Overlying substrate 302 upper surface 303 was a pattern of aluminum lines 304, each having a width 306 of 100 _m and a thickness 308 of 1.7 _m, with a spacing 310 of 2mm separating each line 304. The schematic is not to scale.

Prior to beginning etch of the single crystal silicon substrate 302, a "breakthrough" plasma etch step was carried our using an argon/chlorine plasma source gas, for purposes of removing residual aluminum still present at the mask open area (overlying spaces 310). The breakthrough process conditions were: process chamber pressure 10 mTorr; plasma source power 750 Watts; substrate bias power 175 Watts; argon flow rate 175 sccm; chlorine flow rate 20 sccm; chamber wall temperature 65 _C; cathode temperature 10 _C; etch time 20 min. The etch conditions for each of the eight experiments and the etch results are presented in Table I, below.

TABLE I

Experiment No. _ Process Variable _	1	2	3	4	5	6	7	8
SF_6 Flow (sccm)	70	70	70	70	70	70	70	70
O_2 Flow (sccm)	60	50	60	60	70	60	60	75
HBr Flow (sccm)	--	--	--	--	--	60	60	--
Process Chamber Pressure (mTorr)	20	20	30	30	50	30	50	50
Source Power (W)	700	700	700	700	700	700	700	700
Bias Power (W)	20	20	20	50	70	50	70	70
Cathode Temperature (_C)	10	10	10	10	10	10	10	10
Chamber Wall Temperature (_C)	65	65	65	65	65	65	65	65
Etch Time (min)	20	20	20	20	100	20	20	300
RESULTS								
Depth of Etch into Silicon (_m)	48	56	54	54	208	50	50	370
*Ratio, Line Width At Mask : Etch Base	1.33	»1.33	1.30	1.25	1.35	»1.25	1.52	1.30

*The ratio of line width at the metal mask to line width at the base (bottom) of the etched silicon line is an indication of the amount of undercutting of the etch profile which occurred. The optimum for a vertical trench wall profile would be a ratio of 1.0.

The data in Table 1, above, indicates that an increase in O_2 flow rate to the plasma source gas provides a more vertical trench sidewall profile. This data, in combination with data described subsequently indicates that an increase in the volumetric gas feed ratio of O_2 : SF_6 up to about 1.7 is expected to provide a more vertical profile, depending on other variable nominal values. For the specific ranges of variables presented in Table I and Table II, an increase in the volumetric gas feed ratio of O_2 : SF_6 up to about 1.2 provides a more vertical trench sidewall profile.

A review of the experimental data indicates that a more vertical etched sidewall profile may be achieved by addition of HBr to the plasma feed gas. However, other process variables must be adjusted to accommodate the use of HBr. We have discovered that the addition of HBr to the plasma feed gas may result in more undercutting of the

etch profile (i.e. a higher ratio of line width at the mask to line width at the base of the trench wall), if other process variables are not properly adjusted. This is an unexpected result, as the addition of HBr typically protects the sidewall of the trench during etching, enabling a more vertical trench sidewall profile. In particular, the pressure in the process chamber during etching of the silicon substrate preferably ranges from about 5 mTorr to about 50 mTorr. When HBr is added to the plasma feed gas, a decrease in process chamber pressure from about 50 mTorr to about 20 mTorr provides a more vertical etch sidewall, all other factors held constant. A further decrease below about 20 mTorr results in undercut, reentrant profiles, which are undesirable. In addition to adjustment of the process chamber pressure, we have obtained good results when the volumetric flow rate of SF_6 is about the same as, or slightly less than the flow rate of the HBr.

When HBr is not present in the process gases, an increase in process chamber pressure from about 20 mTorr to about 30 mTorr provides a more vertical trench wall profile, where the ratio of line width at the mask to line width at the base of the trench sidewall is decreased.

An increase in substrate bias from 20 W to 50 W produced a more vertical trench sidewall. Substantially inert diluent gases may be present in the feed gas for purposes of process control; these include argon and helium, by way of example and not by way of limitation.

Figure 3B is a schematic of a cross-sectional view 320 of the etched trench sidewalls 305 and 307 in polysilicon 302 underlying aluminum line 304. This schematic is taken from a photomicrograph of the etched substrate of Experiment No. 5 shown in Table I, where the depth of etch 328 is 208 _m. The remaining aluminum mask thickness 330 was approximately 1.0 _m of the 1.7 _m originally present. The build-up 326 on sidewalls 305 and 307 was analyzed using Electron Diffraction Spectroscopy (EDS). The build- up 326 appears to be mainly silicon, fluorine, and aluminum, with minor amounts of oxygen present. The build-up was subsequently removed by dipping the substrate in a solution of HF in H_2O, where the weight ratio of HF : H_2O was 1 : 100, for a time period of about one minute at ambient temperature. Figure 3C shows the cross-sectional view 340 schematic of Figure 3B after the dip in the HF solution. The

ratio of line width 342 at mask 304 to line width 344 at the base 346 appears for each Experiment No. in the Results section of Table I .

EXAMPLE TWO:

In this Example, 5 experiments were conducted. The film substrate etched was similar to that described with reference to EXAMPLE ONE in terms of the width of the lines and spaces between the lines. However, the line structure was different, as is illustrated in Figure 4A. The film structure 400 included a line 401 resting on the upper surface 403 of single crystal silicon substrate 402. Line 401 had an overall thickness 404 of 5.34 _m, including: a 4,000 _ thick layer of TEOS 404 in direct contact with upper surface 403; a 1,400 _ thick layer of Si_3N_4 406 overlying the TEOS layer 404; a 40,000 _ (4.0 _m) thick masking layer 408 of Al-Cu overlying the Si_3N_4 layer 406; and a second, 8,000 _ thick TEOS layer 410 overlying the Al-Cu masking layer 408.

A pre-clean plasma etch step is optional prior to the etch step described in Table II below. When it is used, it is for purposes of removing debris (such as native oxide) from the

portion of the substrate surface exposed by the mask. In the present Example Two, a pre-clean plasma etch step was carried out prior to etching of the silicon substrate 402. The pre-

clean plasma etch step is typically performed using a plasma generated from a plasma feed gas comprising carbon and fluorine. In this instance the plasma feed gas was CF_4 at about 80 sccm; the process chamber pressure was about 6 mTorr; the plasma source power was about 600 W; the substrate bias power was about 90 W; the cathode temperature was about 10 _C, the process chamber wall temperature was about 55 _C, and the pre-clean etch time was about 10 seconds.

The etch conditions and the etch results for etching of the silicon substrate is provided in Table II below for each of the five etch experiments.

TABLE II

Experiment No. _ Process Variable _	1*	2*	3*	4*	5
SF_6 Flow (sccm)	70	70	70	50	70
O_2 Flow (sccm)	80	80	80	55	70
HBr Flow (sccm)	--	--	--	55	--
Process Chamber Pressure (mTorr)	50	30	30	20	30
Source Power (W)	700	700	700	750	1200
Bias Power (W)	100	150	70	150	400
Substrate Temperature (_C)	10	10	0	0	0
Chamber Wall Temperature (_C)	65	65	65	65	65
Etch Time (min)	60	30	60	60	170
RESULTS					
Depth of Etch into Silicon (_m)	83	82	36	31	428
**Ratio, Line Width At Mask : Etch Base	1.024	1.046	1.024	1.000	_7

* Experiment Nos. 1 through 4 were partial etch processes to study the etch behavior. Experiment No. 5 was a complete, full scale etch process to end point.

**The ratio of line width at the metal mask to line width at the base (bottom) of the etched silicon line is an indication of the amount of undercutting of the etch profile which occurred. The optimum for a vertical trench wall profile would be a ratio of 1.0.

Figure 4B a schematic of a photomicrograph taken from Experiment No. 5, after etching of the film structure 400 shown in Figure 4A, where a portion of Al-Cu masking layer 408 a has been plasma etched, while another portion 408 b has been protected from the etchant plasma. Figure 4B shows the etched structure from Experiment 5 in Table II, where the etch depth 416 into the polysilicon 402 was 428 _m. The line 401 etched into silicon substrate 404 is considerably wider at the Al-Cu masking layer than at the base of the etched silicon 417 (having a Ratio of Line Width At Mask : Etch Base of _7). This is partially the result of the longer etch time, but is attributable principally to a failure to provide sufficient protection for the etched silicon sidewall 413 during the etching

process. The addition of HBr to the plasma feed gas is expected to provide sufficient etched sidewall protection to provide a significantly improved Ratio. The beneficial effect of the addition of HBr is evidenced by the Ratio of 1.0 achieved in Experiment No. 4. Recent experimentation in the etching of deep trenches has indicated that the addition of about 50 sccm to about 80sccm of HBr enables improvement of the Ratio of Line Width At Mask : Etch Base to about 1.2, all other factors held constant.

With regard to the film structure of Experiment No. 5, the thickness of the Al-Cu masking layer 408a (including the first TEOS layer 404, not shown, and the Si_3N_4 layer 406, not shown) remaining after etch of the silicon line 410 was approximately 4.54 _m. The 8,000 _ layer of TEOS 410 was lost, but the Al-Cu masking layer 408 loss was negligible. (The thickness of the protected Al-Cu masking layer structure 401 remained at 5.34 _m.)

Figure 4C is a graph 430 showing the change in silicon etch rate, shown on ordinate 432, as a function of the bias power, shown on abscissa 434, which was applied to the etch structure during etching. Curve 436 shows that for a bias power increase from about 70 W to about 100 W, the etch rate dropped from approximately 1.87 _m per minute to about 1.83 _m per minute (about 2 %).

Figure 4D is a graph 440 showing the change in selectivity (ratio of the etch rate of silicon to the etch rate of the aluminum masking material) on ordinate 442 as a function of the bias power, shown on abscissa 444, which was applied to the etch structure during etching. Curve 446 shows that for the bias power increase from about 70 W to about 100 W, the selectivity decreased from about 180 to about 100 (about 44.5%).

In view of the trends shown in Figures 4C and 4D, it becomes apparent that an increase in the bias power to the substrate has minimal effect of the etch rate of the polysilicon, but can adversely affect the selectivity for etching polysilicon relative to the metal masking layer. As described relative to EXAMPLE ONE, an increase in substrate bias from 20 W to 50 W produced a more vertical trench sidewall.

A review of the experimental data has shown that it is possible to obtain a more vertical etched sidewall when HBr is added to the plasma feed gas, provided other process variables are properly adjusted, as mentioned above.

When a vertical sidewall profile is desired for the etched feature, anisotropic etching is necessary and a bias is applied to the substrate to increase the degree of anisotropic etching. However, an increase in the amount of bias applied decreases the selectivity, so that a thicker mask is required. One skilled in the art can easily determine, for the particular processing apparatus used, the amount of bias which will provide the desired etch profile without an unacceptable reduction in selectivity, based on process requirements.

Preferably, the apparatus used to practice the present invention is adapted to be controlled by a computer. Figure 5 shows a computer 500. Computer 500 comprises a processor 502, memory 504 adapted to store instructions 506, and one or more ports 508. Processor 502 is adapted to communicate with memory 504 and to execute instructions 506. Processor 502 and memory 504 are also adapted to communicate with one or more ports 508. Ports 508 are adapted to communicate with a plasma etch chamber 512. Plasma etch chamber is adapted to carry out process steps in accordance with signals received from processor 502 via ports 508. Preferably, computer 502 can control the composition and feed rate of the plasma source gas, the temperature, the pressure in the chamber, the bias power, the plasma source generation power. Preferably, computer 502 is adapted to receive measurements that describe the condition in the chamber, and adapt the process variables accordingly. This programmed control of process variables enables production of a predetermined device etch profile as required for a given use application.

The above-described preferred embodiments are not intended to limit the scope of the present invention, as one skilled in the art can, in view of the present disclosure expand such embodiments to correspond with the subject matter of the invention claimed below.

CLAIMS

We claim:

1. A method for plasma etching features in a silicon substrate, wherein the depth of etching into said silicon substrate is at least 100 _m, the method including using a metal-comprising masking material in combination with an etchant which provides a non-volatile reaction byproduct which adheres to the masking material, so that a ratio of an etch rate of said masking material to an etch rate of silicon is greater than 40 : 1, and wherein said non-volatile reaction byproduct is sufficiently non-corrosive to features in said substrate that said features remain unharmed by said plasma etching.

2. A method according to Claim 1, wherein said metal-comprising masking material is selected from the group consisting of aluminum, cadmium, copper, chromium, gallium, indium, iron, magnesium, manganese, nickel, and combinations thereof.

3. A method according to Claim 1 or Claim 2, wherein said plasma etchant comprises fluorine.

4. A method according to Claim 3, wherein said metal-comprising masking material is aluminum.

5. A method according to Claim 4, wherein said aluminum-comprising masking material is a combination of aluminum and copper, with other constituents totaling less than about 2.0 % by weight.

6. A method according to Claim 4, wherein said aluminum-comprising masking material is aluminum in combination with less than about 8.0 % by weight magnesium, with other constituents totaling less than about 2.0 % by weight.

7. A method according to Claim 3, or Claim 4, or Claim 5, or Claim 6, wherein said fluorine-comprising plasma etchant is generated from a compound selected from the group consisting of NF_3, CF_4, CHF_3, CH_2F_2, CH_3F, C_4F_8, SF_6, SiF_4, and combinations thereof.

8. A method according to Claim 7, wherein an additional gas selected from the group consisting of O_2, HBr, and combinations thereof is added to said plasma feed gas to assist in etch profile control.

9. A method according to Claim 8, wherein an atomic ratio of oxygen : fluorine in said plasma feed gas ranges from about 0.25 to about 0.50.

10. A method according to Claim 8, wherein the pressure in a process chamber in which said plasma etching is carried out ranges from about 5 mTorr to about 50 mTorr.

11. A method according to Claim 8, wherein a bias power applied to said silicon substrate ranges from about 10 W to about 100 W.

12. A method for plasma etching features in a silicon substrate, wherein the depth of etching into said silicon substrate is at least 100 _m, the method includes using a metal-comprising masking material selected from the group consisting of aluminum, cadmium, copper, chromium, gallium, indium, iron, magnesium, manganese, nickel, and combinations thereof, in combination with a fluorine-comprising plasma etchant generated from a plasma feed gas which comprises a fluorine-containing compound and oxygen.

13. The method of Claim 12, wherein an atomic ratio of oxygen : fluorine in said plasma feed gas ranges from about 0.25 to about 0.50.

14. The method of Claim 12 or Claim 13, wherein said plasma feed gas includes HBr.

15. The method of Claim 14, wherein said method is carried out at a pressure ranging from about 20 mTorr to about 50 mTorr.

16. The method of Claim 12 or Claim 13, wherein said method is carried out at a pressure ranging from about 5 mTorr to about 50 mTorr.

17. An apparatus, comprising:

(a) a memory that stores instructions for:

plasma etching features in a silicon substrate, wherein the depth of etching into said silicon substrate is at least 100 _m, the method including using a metal-comprising masking material in combination with an etchant which provides a non-volatile reaction byproduct which adheres to the masking material, so that a ratio of an etch rate of said masking material to an etch rate of silicon is greater than 40 : 1, and wherein said non-volatile reaction byproduct is sufficiently non-corrosive to features in said substrate that said features remain unharmed by said plasma etching;

(b) a processor adapted to communicate with the memory and to execute the instructions stored by the memory;

(c) an etch chamber adapted to expose the substrate to the etchant in accordance with instructions from the processor; and

(d) a port adapted to pass communications between the processor and the etch chamber.

18. An article of manufacture comprising:

a recordable medium having recorded thereon a plurality of programming instructions for use to program an apparatus which controls an etch process to proceed by the method of Claim 1 or Claim 12.

19. An article of manufacture comprising:

a recordable medium having recorded thereon a plurality of programming instructions for use to program an apparatus which controls an etch process to proceed

by the method of Claim 1 or Claim 12.

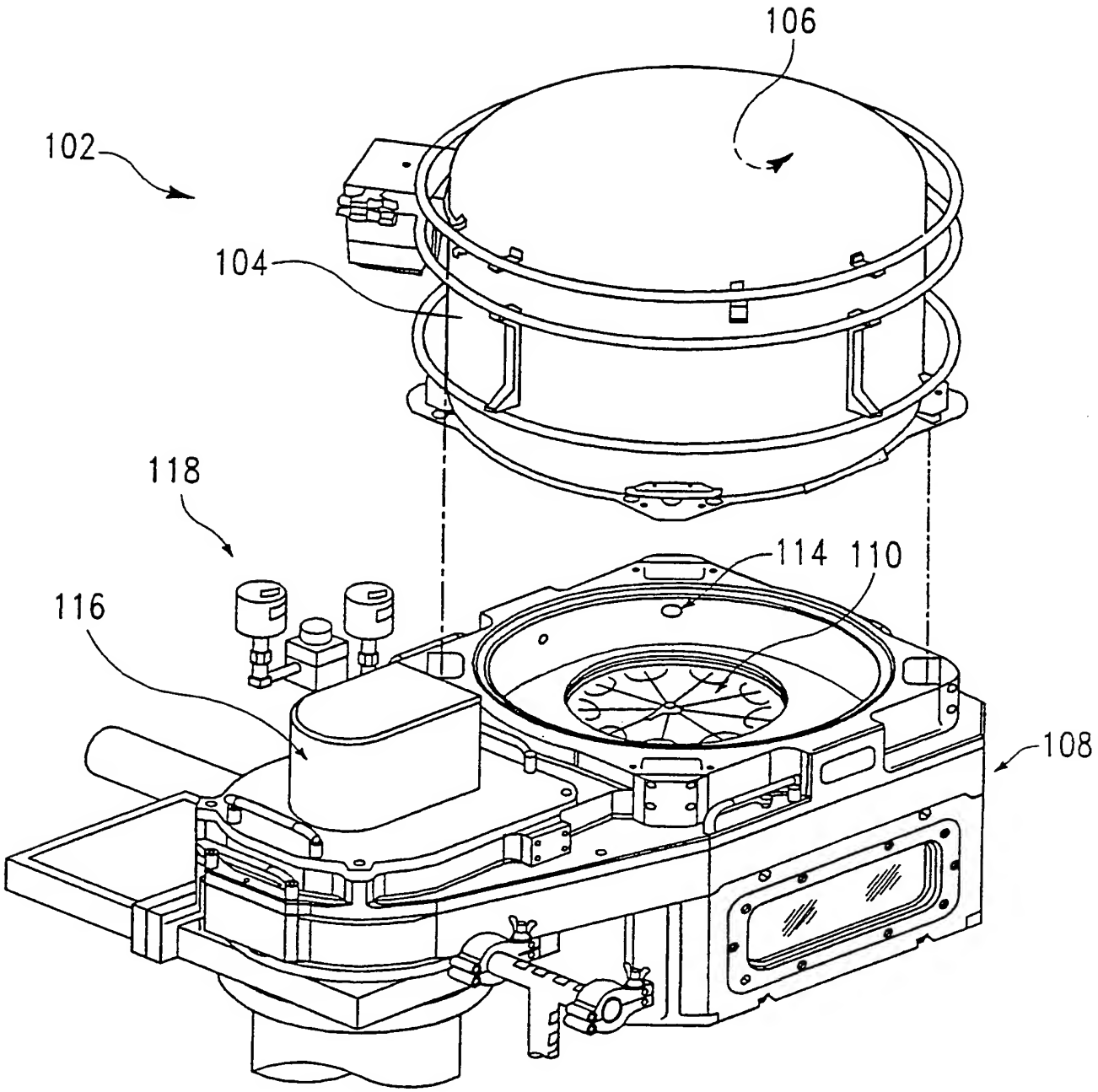

FIG. 1 (PRIOR ART)

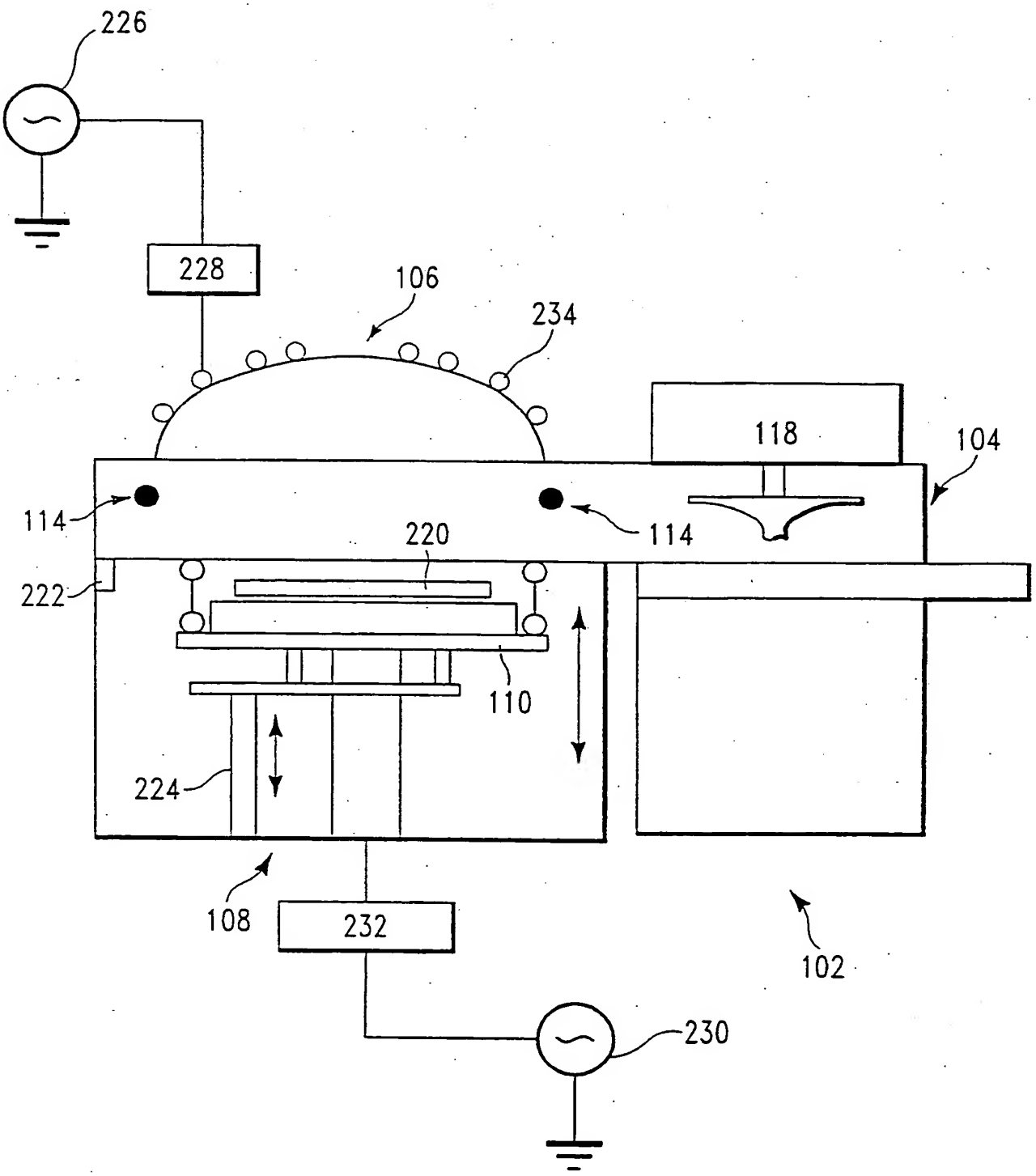

FIG. 2 (Prior Art)

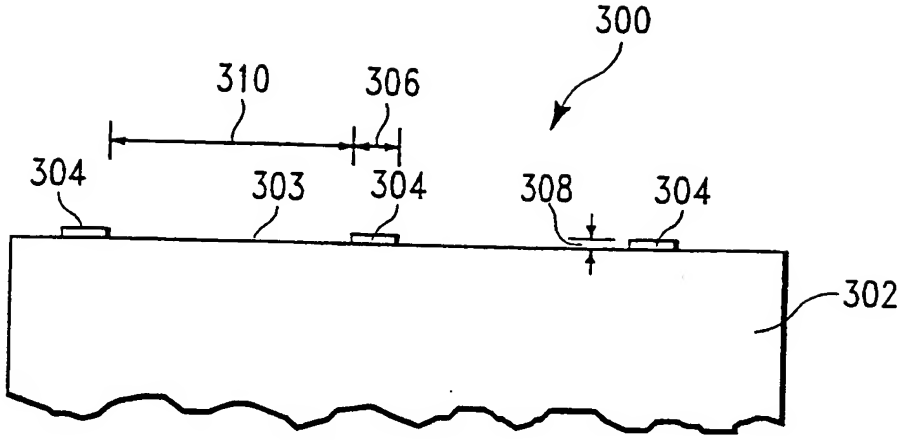

FIG. 3A

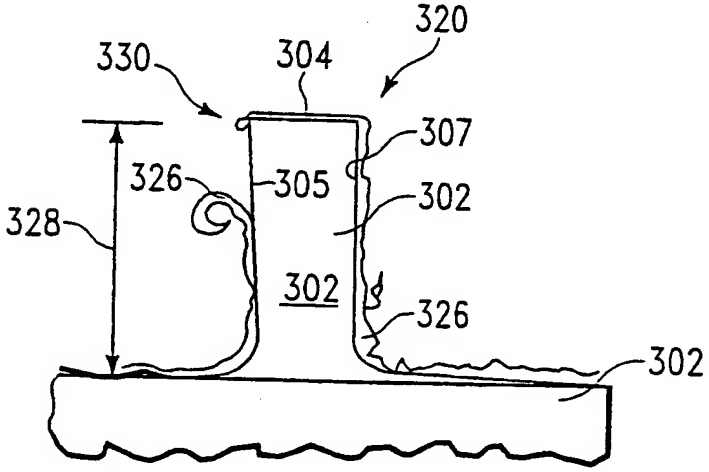

FIG. 3B

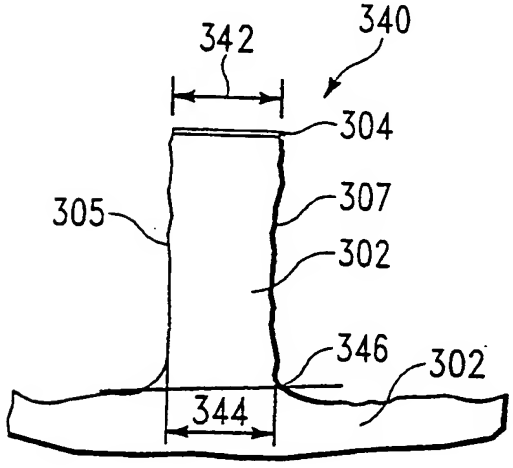

FIG. 3C

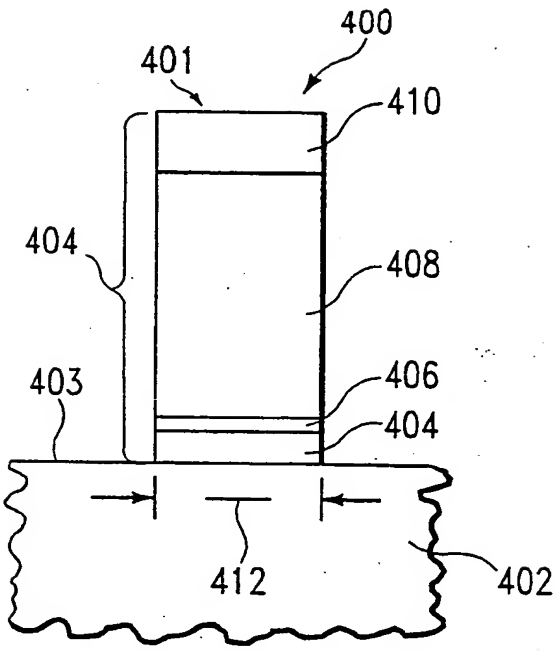

FIG. 4A

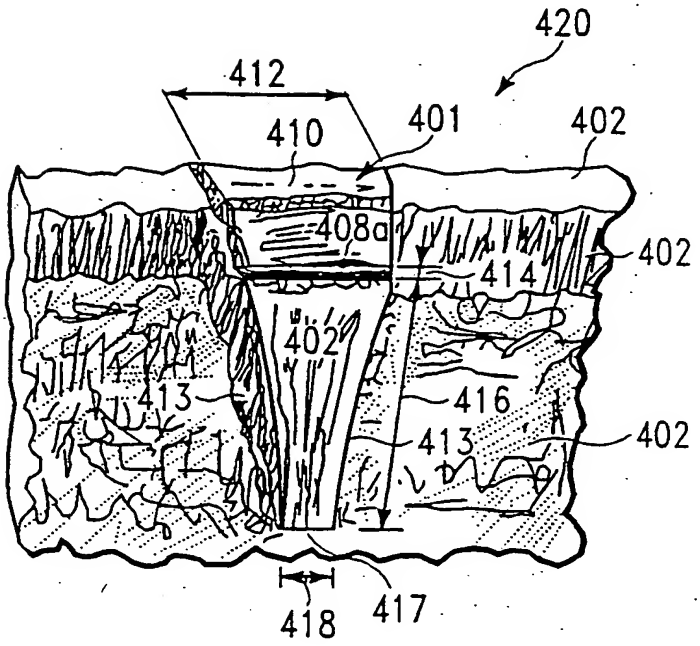

FIG. 4B

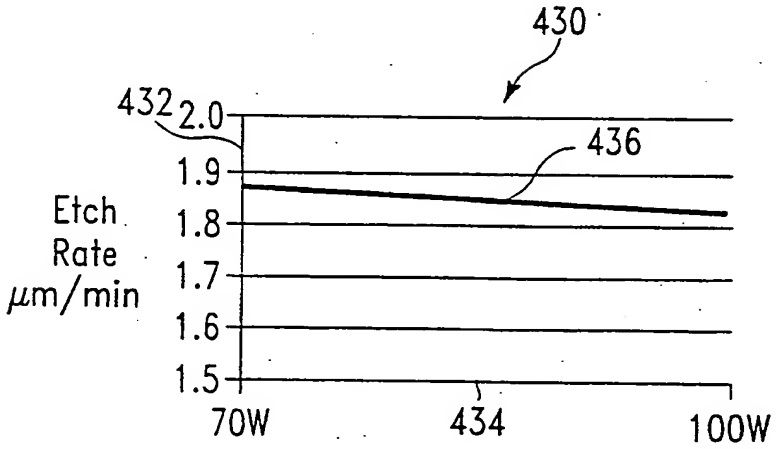

FIG. 4C

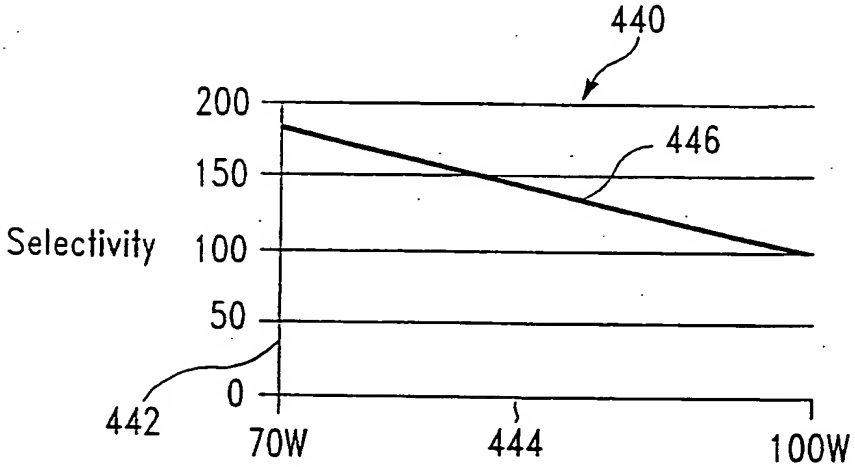

FIG. 4D

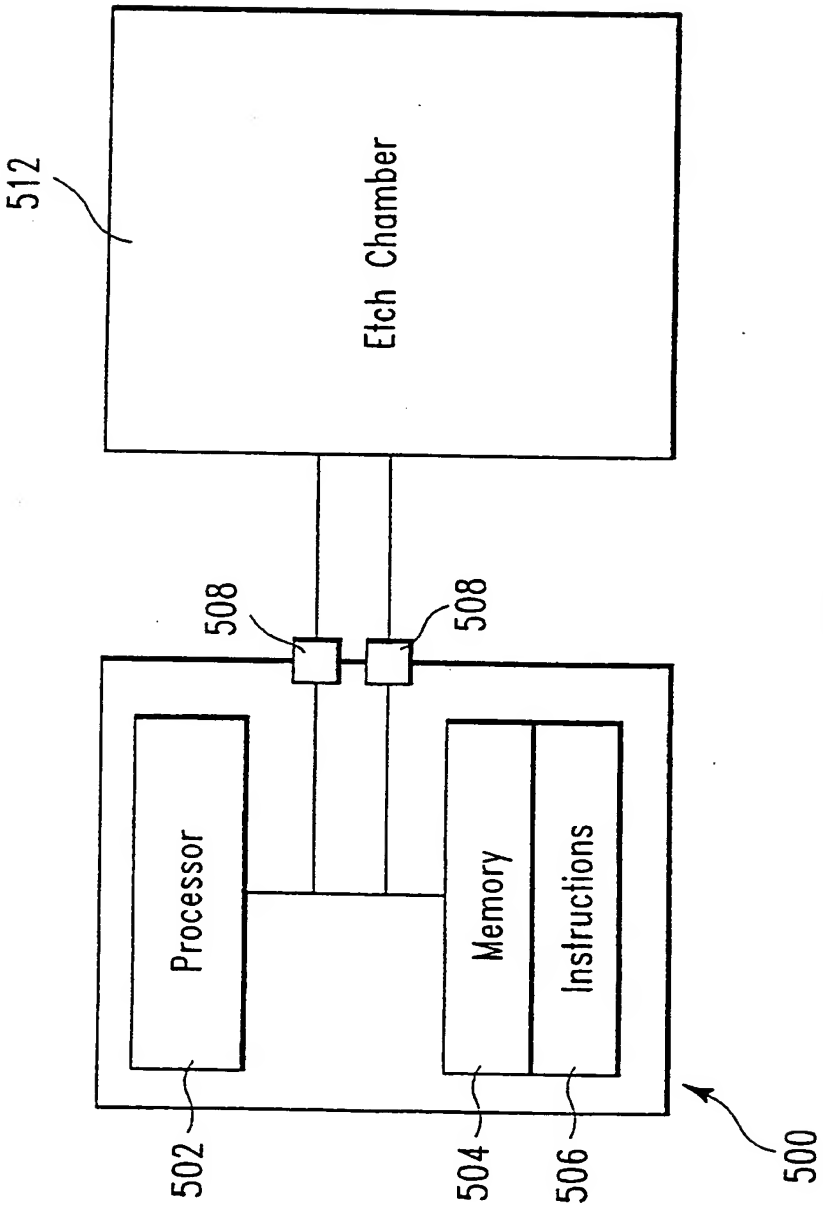

FIG. 5

INTERNATIONAL SEARCH REPORT

Inter[illegible]ication No
PCT/US 00/34684

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/308

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 12, 26 December 1996 (1996-12-26) & JP 08 203875 A (FUJI ELECTRIC CO LTD), 9 August 1996 (1996-08-09)	1-4,7, 12,13,16
Y	abstract	5-11

X	US 5 536 364 A (YOSHIDA ET AL) 16 July 1996 (1996-07-16)	1-4,7, 12,13,16
Y	claims; table 1	5,6

X	US 5 368 685 A (KUMIHASHI ET AL) 29 November 1994 (1994-11-29) figures 3,9	17-19

Y	US 5 605 603 A (GRIMARD ET AL) 25 February 1997 (1997-02-25) abstract	7-11

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 April 2001	16. 04. 01

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax (+31–70) 340–3016	Gori, P

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99 36947 A (DERONELLAS ET AL) 22 July 1999 (1999-07-22) page 9, last line -page 11, line 6; claims	1-16
A	EP 0 581 280 A (CANON) 2 February 1994 (1994-02-02) page 6, line 20 - line 29	1-16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 00/34684

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

XCID: <WO___0147005A1_I_>

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Present claim 1 relates to a methodl defined by reference to a desirable characteristic or property, namely the use of a masking material in combinaiton with an etchant providing a protective/passivating non volatile reaction product so that the selectivity is higher than 40.

The claim covers all methods having this characteristic or property, whereas the application provides support within the meaning of Article 6 PCT and/or disclosure within the meaning of Article 5 PCT for only a very limited number of such methods. In the present case, the claims so lack support, and the application so lacks disclosure, that a meaningful search over the whole of the claimed scope is impossible. Independent of the above reasoning, the claims also lack clarity (Article 6 PCT) in that an attempt is made to define the method by reference to a result to be achieved. Again, this lack of clarity in the present case is such as to render a meaningful search over the whole of the claimed scope impossible. Consequently, the search has been carried out for those parts of the claims which appear to be clear, supported and disclosed, namely those parts relating to a method of etching silicon with a mask of aluminium with a plasma of a fluorine-containing gas and oxygen, possibly in admixture with HBr, as disclosed in Example 1.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter... ...plication No
PCT/US 00/34684

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